

A Transistorized Formant-Type Synthesizer

As part of the program of using digital methods for speech research, one of the peripheral instruments needed is a formant-type synthesizer which will generate high quality synthetic speech. The synthesizer will be driven from the digital spectrum manipulator (DSM). This involves signal conversions since the DSM normally receives and stores successive time-quantized samples of the outputs of a filter bank. Spectrum information in this form can be used directly to drive a channel-vocoder-type of synthesizer, but does not meet the input needs of a formant-type synthesizer. In initial experiments, the formant control signals will be generated by hand methods, which means in effect tracing the formants on the DSM display and storing this time-frequency data for use as control signals. Computer routines to track the formants and so provide the control signals will follow.

The development of a transistorized formant-type synthesizer has been started. The first phase, namely, the design and construction of voltage-controlled formant generators has been completed. The formant generator is, in effect, an analog simulation of a second-order differential equation, and so given a decreasing, exponentially damped wave. The formant generator circuit diagram is shown in Figure 1.

The formant frequency range is determined by the capacitors in the two integrators within the loop. The formant frequency is then varied by changing the amount of feedback at two points within the loop, which requires a method of achieving a variable

resistance of wide range. The approach used was pulse-duration modulation (PDM). With this method, the input signal is used to control the pulse duration of a constant repetition rate pulse signal, which in turn removes a low resistance shunt from the output. The repetition rate of the pulse signal is much higher than the signal frequency, permitting the PDM signal to be removed by a filter at the output, leaving its envelope as the formant-frequency signal. A pulse repetition rate of 20 kc was dictated by filter considerations and the comparatively low formant frequency. In practice, the integrators within the loop have a filtering effect on the switched signal and a 10 kc filter at the output takes care of the remaining 20 kc switching signal, leaving a clean formant frequency wave.

The circuits are shown in Figures 1 and 2. The dc control voltage input (from a D/A converter) varies the pulse duration of the 20 kc pulse signal. The bi-directional transmission gates are then switched by the output of the pulse width generator. The circuitry for this dc controlled pulse width generator uses an 80 kc crystal oscillator divided down to 20 kc and shaped to 0.25 μ sec pulses to drive the ramp generator. The ramp signal is then used to drive the dc input of a Schmitt trigger, while the dc control voltage sets its threshold. An inverter and level shifting stage is used to drive the bi-directional transmission gates within the loop of the formant generator. The bi-directional gates are normally conducting, thus permitting no signal to appear at the output. When they are switched by the variable pulse width signals, they bias the gates off, thus permitting signal transmission. The gates themselves have an attenuation factor of 60 db when turned on. Each gate has an adjustment for differences in components, power supplies and offset produced by the operational amplifiers; these adjustments eliminate "thump," i.e., shifts in the base line when changing formant frequency.

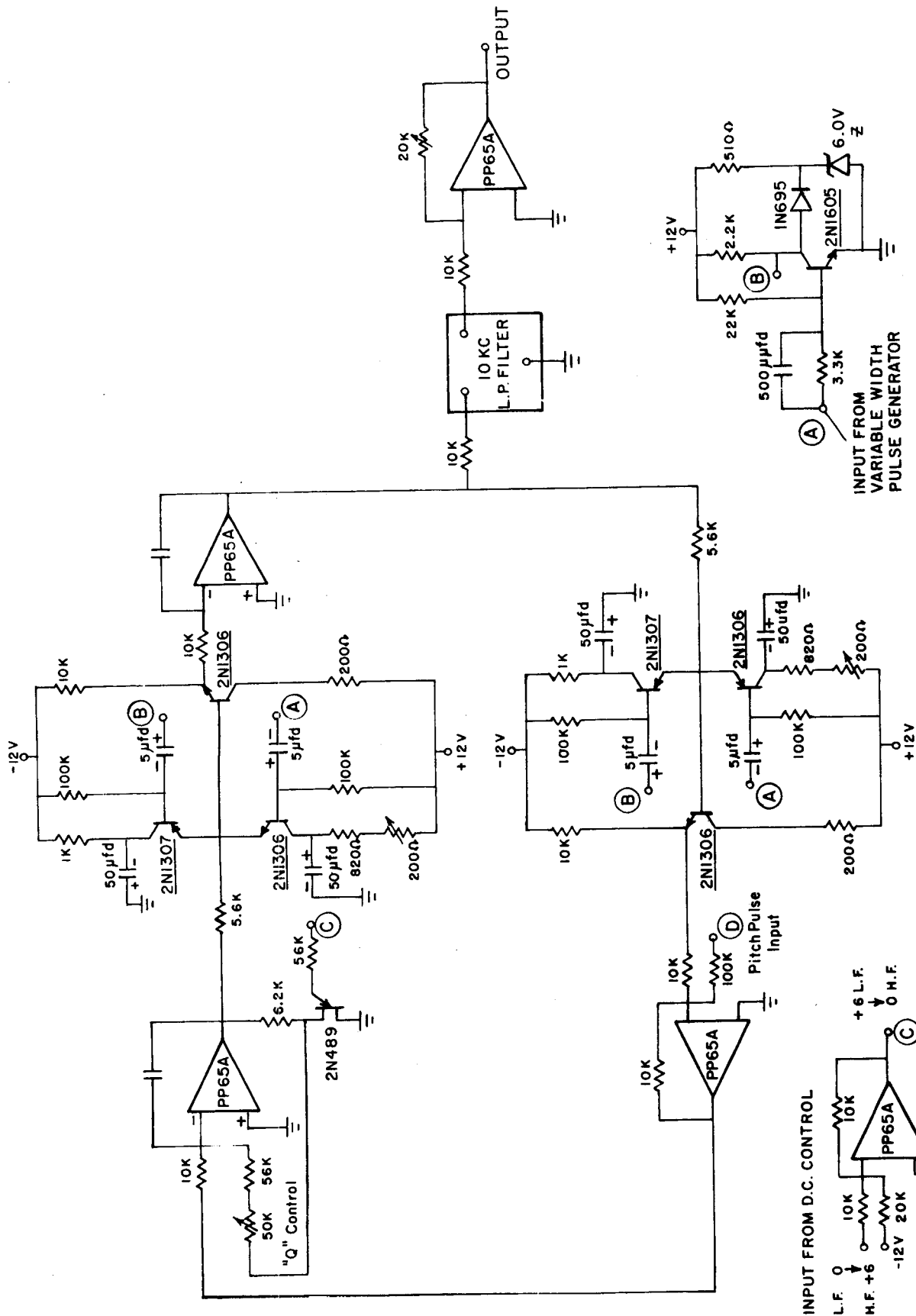
The circuit displays an almost linearly rising Q , i.e., a constant bandwidth characteristic with increasing formant frequency. Some compensation was needed at the lower end of the formant frequency vs. Q -characteristic curve. This was accomplished by the use of a unijunction transistor circuit as a variable resistance in the feedback path. This effectively boosted the Q at the lower formant frequencies.

Curves have been made of formant frequency vs dc control voltages. One of them is shown in Figure 3. They display a 1 to 2% linearity characteristic over frequency ranges fully adequate for each of the first three formants.

We have recently begun work on other circuits required for the system.

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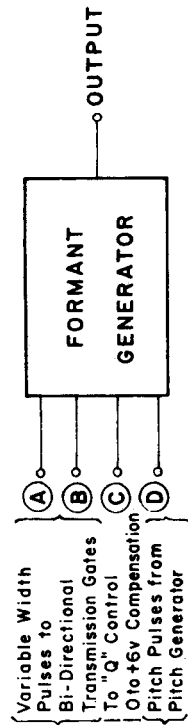
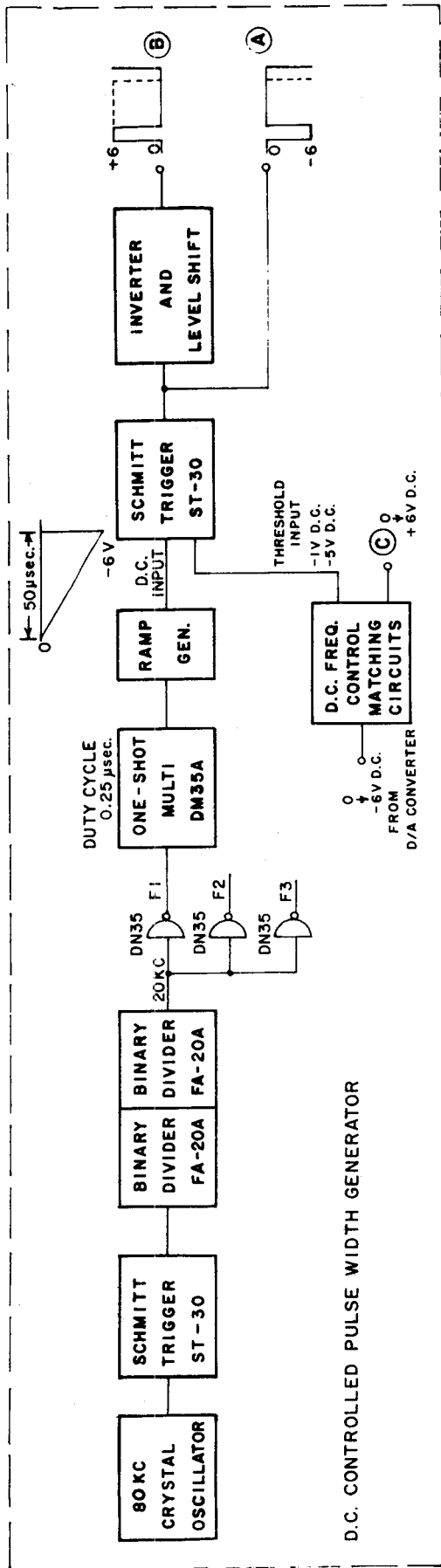
ANALOG SIMULATION OF A FORMANT GENERATOR



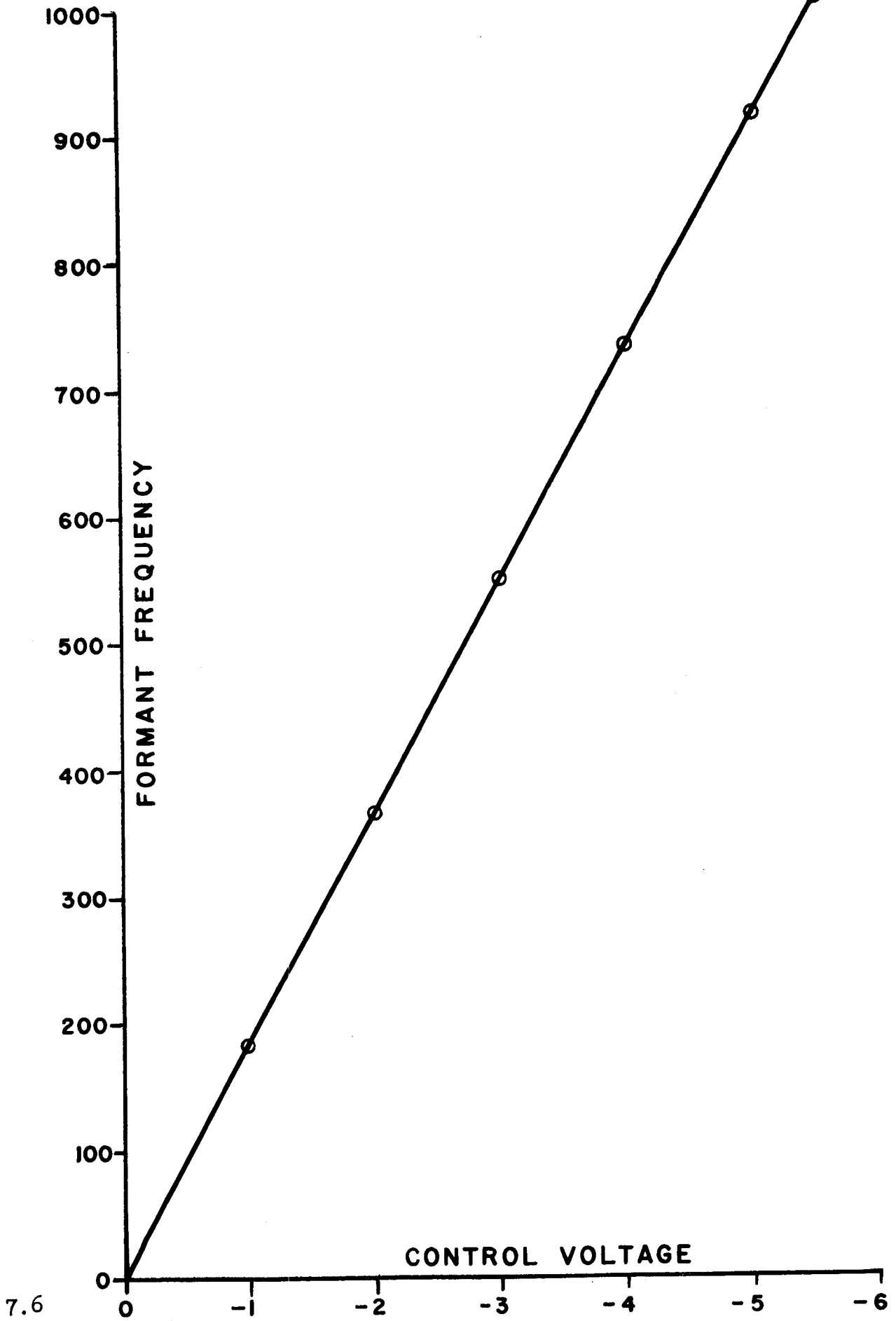
PULSE INVERTER

"Q" COMPENSATION

BLOCK DIAGRAM OF FORMANT GENERATOR FREQUENCY CONTROL CIRCUITS



FIRST-FORMANT GENERATOR



7.6

FIG. 3